## Short summery of all hardware platforms

This is a short description of the different hardware. The SW drivers etc. is described in the book.

**HW_CASE_1A:**

| Slave Descriptor | Address Range | Size | Attributes |
|---|---|---|---|
| jtag_uart | 0x00009000 - 0x00009007 | 8 | printable |
| onchip_ram | 0x00004000 - 0x00007FFF | 16384 | memory |

*Figure 1: HW_CASE_1A, Memory Map*

**HW_CASE_1C:**

| Slave Descriptor | Address Range | Size | Attributes |
|---|---|---|---|
| jtag_uart | 0x00009020 - 0x00009027 | 8 | printable |
| pio_in_key | 0x00009010 - 0x0000901F | 16 | |
| pio_out_led | 0x00009000 - 0x0000900F | 16 | |
| onchip_ram | 0x00004000 - 0x00007FFF | 16384 | memory |
| sysid | 0x00000000 - 0x00000007 | 8 | |

*Figure 2: HW_CASE_1C, Memory Map*

**HW_CASE_2:**

| Slave Descriptor | Address Range | Size | Attributes |
|---|---|---|---|
| jtag_uart | 0x08009018 - 0x0800901F | 8 | printable |
| sysid | 0x08009010 - 0x08009017 | 8 | |
| altpll | 0x08009000 - 0x0800900F | 16 | |
| onchip_ram | 0x08004000 - 0x08007FFF | 16384 | memory |
| sdram_controller | 0x04000000 - 0x07FFFFFF | 67108864 | memory |

*Figure 3: HW_CASE_2, Memory Map*

Sometimes it is also problem with “system timestamp mismatch”, please ignore this problem. This issue has no design impact.

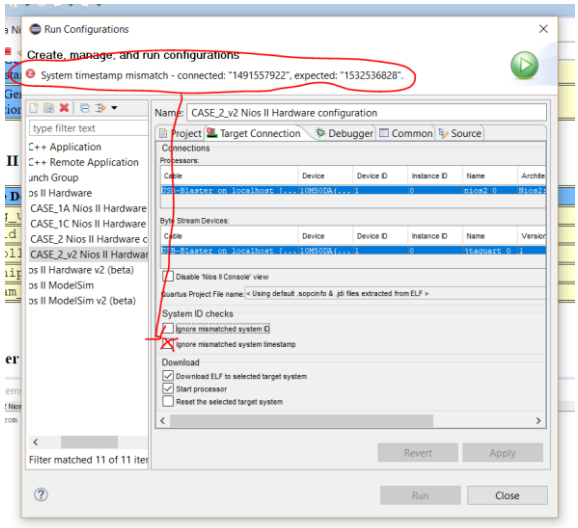


*Figure 4: Tick the [Ignore mismatched System timestamp] field.*

**HW_CASE_3:**

Used for CASE_3A and CASE_3B

| Slave Descriptor | Address Range | Size | Attributes |
|---|---|---|---|
| sysid | 0x00009018 - 0x0000901F | 8 | |
| jtag_uart | 0x00009010 - 0x00009017 | 8 | printable |
| TIMER_HW_IP_0 | 0x00009000 - 0x0000900F | 16 | |
| onchip_ram | 0x00004000 - 0x00007FFF | 16384 | memory |

*Figure 5: HW_CASE_3, Memory Map*

**HW_CASE_4_E and CASE_4_F:**

The difference between them is the CPU as shown in next figure.

| | Nios II/e | Nios II/f |
|---|---|---|
| **Summary** | **Resource-optimized 32-bit RISC** | **Performance-optimized 32-bit RISC** |
| **Features** | **JTAG Debug**<br>**ECC RAM Protection** | **JTAG Debug**<br>**Hardware Multiply/Divide**<br>**Instruction/Data Caches**<br>**Tightly-Coupled Masters**<br>**ECC RAM Protection**<br>**External Interrupt Controller**<br>**Shadow Register Sets**<br>**MPU**<br>**MMU** |
| RAM Usage | 2 + Options | 2 + Options |

*Figure 6: Nios economy (CASE_4_E ) and NIOS fast (CASE_4_F)*

The NIOS economy has no cache.

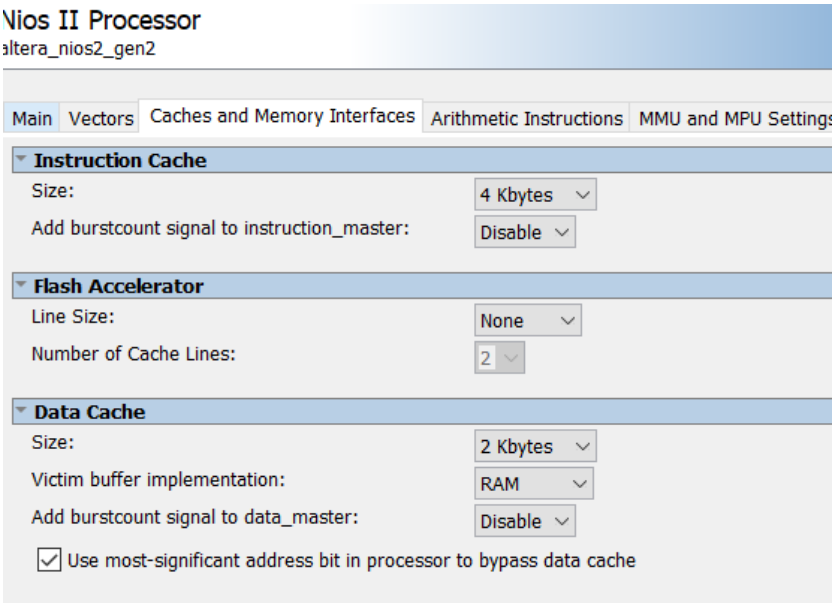


*Figure 7: Nios II fast has data and instruction cache*

Used for CASE_4.

| Slave Descriptor | Address Range | Size | Attributes |
|---|---|---|---|
| jtag_uart | 0x08009018 - 0x0800901F | 8 | printable |
| sysid | 0x08009010 - 0x08009017 | 8 | |
| TIMER_HW_IP_0 | 0x08009000 - 0x0800900F | 16 | |
| onchip_ram | 0x08004000 - 0x08007FFF | 16384 | memory |
| sdram_controller | 0x04000000 - 0x07FFFFFF | 67108864 | memory |
| altpll | 0x00000000 - 0x0000000F | 16 | |

*Figure 8: Memory map for HW_CASE_4_E and HW_CASE_4_F*

When you run CASE_4_F do not close the window "OpenCore Plus Status". It is not a free IP component, but we can use it if we have a connection to it and it will only run for some time.

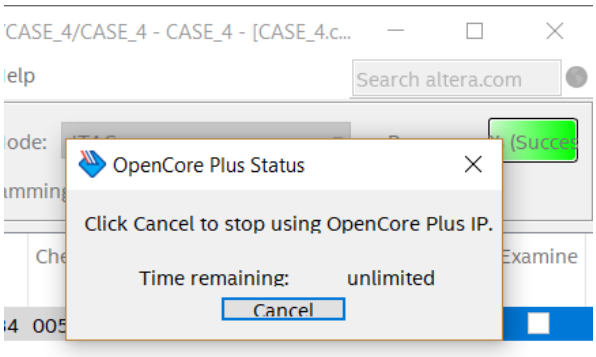


*Figure 9: Do not close down the "OpenCore Plus Status"*

**CASE_5A:**

| Slave Descriptor | Address Range | Size | Attributes |
|---|---|---|---|
| jtag_uart | 0x08009048 - 0x0800904F | 8 | printable |
| sysid | 0x08009040 - 0x08009047 | 8 | |
| pll | 0x08009030 - 0x0800903F | 16 | |
| TIMER_HW_IP_0 | 0x08009020 - 0x0800902F | 16 | |
| pio_out_leds | 0x08009010 - 0x0800901F | 16 | |
| pio_in_buttons | 0x08009000 - 0x0800900F | 16 | |
| onchip_ram | 0x08004000 - 0x08007FFF | 16384 | memory |
| sdram_controller | 0x04000000 - 0x07FFFFFF | 67108864 | memory |

*Figure 10: HW_CASE_5A, Memory Map*

**CASE_5B:**

| Slave Descriptor | Address Range | Size | Attributes |
|---|---|---|---|
| jtag_uart | 0x08009048 - 0x0800904F | 8 | printable |
| sysid | 0x08009040 - 0x08009047 | 8 | |
| pll | 0x08009030 - 0x0800903F | 16 | |
| TIMER_HW_IP_0 | 0x08009020 - 0x0800902F | 16 | |
| pio_out_leds | 0x08009010 - 0x0800901F | 16 | |
| pio_in_buttons | 0x08009000 - 0x0800900F | 16 | |
| onchip_ram | 0x08004000 - 0x08007FFF | 16384 | memory |
| sdram_controller | 0x04000000 - 0x07FFFFFF | 67108864 | memory |

*Figure 11: HW_CASE_5B, Memory Map*

**CASE_GOLD:**

It is the end design for the practical training in this book, targeted to DE10-Litle evaluation board. It also includes key components, such as PIO, Analog and SPI interfaces (interface to accelerometer). It also includes one hardware based Real-Time kernel in hardware. The total embedded system fits easy in one small and cheap FPGA device.
The hardware HW_CASE_GOLD will be used for the real-time, analog and Bluetooth cases.

| Slave Descriptor | Address Range | Size | Attributes |
|---|---|---|---|
| accelerometer_spi_0 | 0x080916F0 - 0x080916F1 | 2 | |
| jtag_uart | 0x080916E8 - 0x080916EF | 8 | printable |
| rs232_0 | 0x080916E0 - 0x080916E7 | 8 | |
| sysid_qsys_0 | 0x080916D8 - 0x080916DF | 8 | |
| modular_adc_0_sequencer_csr | 0x080916D0 - 0x080916D7 | 8 | |
| TIMER_HW_IP_0 | 0x080916C0 - 0x080916CF | 16 | |
| pll_0 | 0x080916B0 - 0x080916BF | 16 | |
| pll_1 | 0x080916A0 - 0x080916AF | 16 | |
| pio_leds_out | 0x08091690 - 0x0809169F | 16 | |
| pio_buttons_in | 0x08091680 - 0x0809168F | 16 | |
| pio_switches_in | 0x08091670 - 0x0809167F | 16 | |
| pio_0 | 0x08091660 - 0x0809166F | 16 | |
| DE10_Lite_SSD_IP_0 | 0x08091640 - 0x0809165F | 32 | |
| DE10_Lite_Arduino_IP_0 | 0x08091600 - 0x0809163F | 64 | |
| modular_adc_0_sample_store_csr | 0x08091400 - 0x080915FF | 512 | |
| sierra_0 | 0x08091000 - 0x080913FF | 1024 | |
| onchip_ram | 0x08088000 - 0x0808FFFF | 32768 | memory |
| DE10_Lite_VGA_IP_0 | 0x08000000 - 0x0807FFFF | 524288 | |
| sdram_controller | 0x04000000 - 0x07FFFFFF | 67108864 | memory |

*Figure 12: HW_CASE_GOLD, Memory Map*

**An example of the software projects in Nios II Embedded Design Suite**

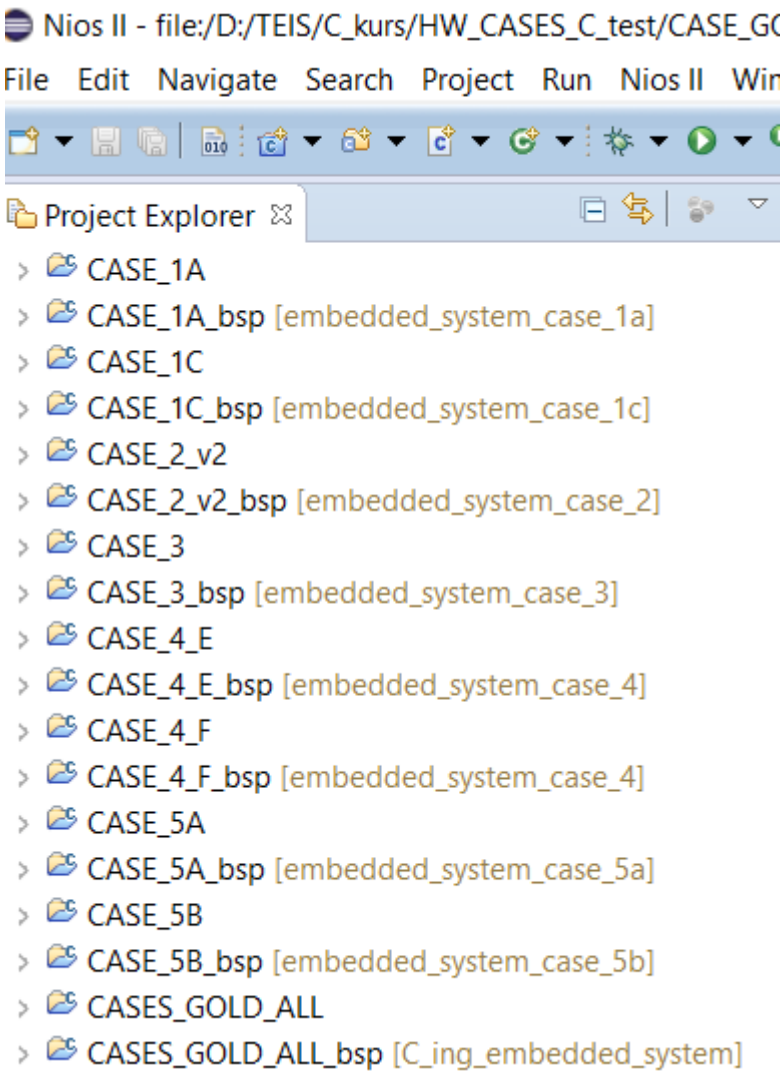


*Figure 13: Example of the CASE projects*